

Remarks

Information Disclosure Statements

An Information Disclosure Statement is being filed concurrently with this Amendment. In addition, Information Disclosure Statements were previously filed on April 30, 2004, September 30, 2004 and December 3, 2004. Despite a previous request and payment of the requisite fees, Applicant has not received initialed copies of the PTO SB/08 forms submitted with the Information Disclosure Statements indicating that the references cited therein were considered by the Examiner. It is again requested that initialed copies of the PTO Forms SB/08 be provided to Applicant.

Claim Rejections Under 35 USC 103(a)

Claims 34-35, 39-41, 43, 49 and 51 have been rejected under 35 USC 103(a) as being unpatentable over Fjelstad et al. (US Patent No. 5,615,824) in view of Maruyama et al. (US Patent No. 6,661,247).

Claim 38 has been rejected under 35 USC 103(a) as being unpatentable over Fjelstad et al. (US Patent No. 5,632,631) and Maruyama et al. (US Patent No. 6,661,247) in view of Sugiyama et al. (US Patent No. 4,766,666).

Claims 40-41 and 50 have been rejected under 35 USC 103(a) as being unpatentable over Fjelstad et al. (US Patent No. 5,632,631) and Maruyama et al. (US Patent No. 6,661,247) in view of Kazle (US Patent No. 5,936,847).

The rejections under 35 USC §103 are traversed for reasons to follow.

Reading of Claims

A reading of the rejected claims on the drawings and specification is as follow.

34. A method for fabricating an interconnect (10-Figure 1, page 9, lines 6-30) for electrically engaging a semiconductor component (18-Figure 3B) with at least one bumped contact (14B-Figure 7G) having a radius (R-Figure 7G) comprising:

providing a substrate (14B-Figure 7A, page 18, line 33 to page 19, line 3) having a surface (26B-Figure 3C);

forming a plurality of leads (22B-Figure 7C, page 19, lines 10-14) on the surface (26B-Figure 3C) configured to electrically engage and support the bumped contact (Figure 3B, page 4, lines 18-21), the leads having terminal portions (Figure 7G) and support portions (Figure 7G);

forming a recess (20B-Figure 7F, page 21, lines 10-14) in the surface configured to cantilever the terminal portions over the recess with the support portions on the surface supporting the terminal portions (Figure 7G) for movement within the recess during electrical engagement of the bumped contact (page 13, lines 5-8); and

shaping the terminal portions with a curvature (Figure 7G) approximately equal to the radius of the bumped contact (page 21, lines 15-20).

35. The method of claim 34 further comprising forming outer layers (46B-Figure 7B and 3D, page 19, lines 4-9 of the specification) on the terminal portions configured to provide a non bonding surface for the bumped contact.

38. The method of claim 34 wherein the substrate comprises a semiconductor material (page 10, line 4) and

the forming the recess step comprises etching (page 16, line 30).

39. A method for fabricating an interconnect (10-Figure 1, page 9, lines 6-30) for electrically engaging a semiconductor component (18-Figure 2C) having at least one bumped contact (14B-Figure 7G) having a shape (page 13, line 2) comprising:

providing a substrate (14B-Figure 7A, page 18, line 33 to page 19, line 3) having a surface (26B-Figure 3C);

forming a metal layer (leads 22B-Figure 7C, page 19, lines 10-14) on the surface (26B-Figure 3C);

forming a plurality of leads (leads 22B-Figure 7C, page 19, lines 10-14) on the substrate configured to electrically engage and support the bumped contact (Figure 3B, page 4, lines 18-21), the leads having terminal portions (Figure 7G) and support portions (Figure 7G), each terminal portion having at least one projection (blade 28B-Figure 7B) configured to penetrate the bumped contact;

forming a recess (20B-Figure 7F, page 21, lines 10-14) in the surface configured to cantilever the terminal portions over the recess with the support portions on the surface supporting the terminal portions for movement within the recess during electrical engagement of the bumped contact (page 13, lines 5-8); and

shaping the terminal portions with a curvature (Figure 7G) matching the shape of the bumped contact (page 13, lines 1-5, page 21, lines 15-20).

40. The method of claim 39 wherein the shaping step comprises pressing the leads with a tool (page 21, lines 18-20).

41. The method of claim 39 wherein the shaping step comprises heating the leads (page 21, lines 18-20).

43. The method of claim 39 further comprising forming a connecting segment (40B-Figure 7F, page 19, lines 11-14) on the substrate electrically connecting the leads, a conductive via (42B-Figure 7E, page 19, line 15 to page 20, line 31) in the substrate in electrical communication with the connecting segment and a contact (38B-Figure 7F, page 20, line 32 to page 21, line 9) on the substrate in electrical communication with the conductive via.

49. A method for fabricating an interconnect (10-Figure 1, page 9, lines 6-30) for electrically engaging a semiconductor component (18-Figure 2C page 9, lines 6-30) having a plurality of bumped contacts (16-Figure 2C page 9, lines 6-30) on comprising:

providing a substrate (14B-Figure 7A, page 18, line 33 to page 19, line 3);

forming a plurality of interconnect contacts (14B-Figure 7G, page 18, line 2 to page 21 line 20) on the substrate configured to electrically engage the bumped contacts (page 9, line 26), each interconnect contact comprising a plurality of leads (leads 22B-Figure 7C, page 19, lines 10-14) having terminal portions (30A-Figure 2B, page 10, line 33) and projections (blades 28B-Figure 7B, page 19, lines 4-5 described as projections on page 4, line 25) on the terminal portions configured to penetrate the bumped contacts (page 12, lines 31-34);

forming outer layers (46B-Figure 7B and 3D, page 19, lines 4-9) on the terminal portions and projections configured to provide non-bonding surfaces for the bumped contacts (page 13, line 27, to page 14, line 2)

forming a plurality of recesses (20B-Figure 7F, page 21, lines 10-14) in the substrate proximate to the leads configured to cantilever the terminal portions of the leads for movement within the recesses during the electrical engagement (page 12, lines 2-5); and

shaping the terminal portions (Figure 7G) to match a shape of a bumped contact (**page 13, lines 1-5, page 21, lines 15-20**).

50. The method of claim 49 wherein the outer layers comprise a conductive polymer (**page 14, lines 1-2 of the specification**).

51. The method of claim 49 wherein the projections comprise blades (**blades 28B-Figure 7B, page 19**).

Argument

The rejections under 35 USC §103(a) are traversed as the priority date of the present application (03/10/1999) precedes the priority date of Maruyama et al. (03/16/1999). In this regard, the present application is a division of serial no. 09/266,237 filed on 03/10/1999, whereas Maruyama et al. is a division of serial no. 09/268,338 filed on 03/16/1999.

Maruyama et al. is also a continuation-in-part of serial no. 09/009,261 filed on 01/20/1998. However, a continuation-in-part does not receive the earlier priority date for new matter. Maruyama et al. was cited for teaching that "various sizes of the bumps are used to shape the leads (col. 7, lines 18-19)". However, this sentence may not be entitled to the earlier filing date. In rejecting claims under 35 USC §103, the Examiner bears the initial burden of presenting a prima facie case of obviousness. In re Oetiker, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992). Accordingly, the burden is on the Examiner to demonstrate the quoted sentence is entitled

to a priority date earlier than that of the present application.

The rejections under 35 USC §103(a) are further traversed because the combination of references does not disclose all of the features of the present invention as required by MPEP 2142, 2143. A first undisclosed feature recited in independent claims 34, 39 and 49 is the step of "shaping the terminal portions with a curvature approximately equal to the radius of the bumped contact". Dependent claim 40 recites that "the shaping step comprises pressing the leads with a tool". Dependent claim 41 recites "the shaping step comprises heating the leads".

The sentence at column 7, lines 18-19 of Maruyama et al. was cited as teaching the presently claimed "shaping" step. However, Applicant disputes that the cited sentence in Maruyama et al. teaches a "shaping" step. In this regard, the cited sentence states:

"Further, as mentioned above, each connection portion 24A with which a respective one of the bumps 2 is connected is deformable. Accordingly, even if the sizes (heights) of the bumps 2 vary, as a result of the connection portions 24A being deformed, the variation of the heights of the bumps 2 is accommodated".

Deforming the connection portions 24A (Figure 2) to accommodate height variations in bumps 2 (Figure 2) is not the same as shaping with a radius of curvature corresponding to the bumps as presently claimed. In Figure 2 of Maruyama et al. the connection portion 24A does not have a radius of curvature matching the bump 2.

Under 35 USC §103(a) obviousness is to be assessed from the point of view of one skilled in the art at the time of the invention. It is submitted that absent the teachings of the present disclosure, one skilled in the art at the time of the present invention would not interpret

the above quoted passage as teaching the shaping of leads with a radius of curvature, nor the shaping of leads using a tool, nor the shaping of leads using heat.

A second undisclosed feature recited in independent claims 39 and 49 is "each terminal portion having at least one projection configured to penetrate the bumped contact". Antecedent basis for the term "projection" is provided on page 4, lines 24-26, and on page 12, lines 31-34 of the specification. In addition, penetrating projections in the form of blades 28B are shown in Figures 7G-7B. Independent claim 49 also states that the projections are configured to penetrate oxide layers. Antecedent basis for this recitation is contained on page 4, lines 25-26 of the specification.

The asperities 30 in Figure 3 of Fjelstad et al. were cited as teaching a penetrating structure. As stated in the Office Action: "30 digs into the surface of ball 72". However, Applicant is unable to locate any disclosure in Fjelstad et al. that the asperities 30 perform a "penetrating" or "digging" function. In Figure 3 of Fjelstad et al., there is no penetration of the asperities 30 into the balls 72.

Applicant would further argue that one skilled in the art at the time of the invention would have no incentive to combine Fjelstad et al. and Maruyama et al. in the manner of the Office Action. The Office Action states the incentive for the proposed combination as: "for the purpose of positively connecting the bumps to the terminal portions to improve reliability of the test". However, the proposed incentive, rather than being from the point of view of one skilled in the art at the time of the invention, appears to

have been reverse engineered to support the 35 USC §103 rejections.

Further, in regard to the proposed combination of Fjelstad et al. and Maruyama et al., if the contacts 20 in Figure 3 of Fjelstad et al. were to be shaped with a radius of curvature, the flat surfaces of the asperities 36, rather than the edges thereof, would contact the ball 72. The resultant electrical connections would be less reliable, rather than more reliable. The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification, In re Fritch, 972 F.2d 1260, 1266, 12 USPQ2d 1780, 1783-1784 (Fed. Cir. 1992).

A third undisclosed feature recited in independent claim 49 is an outer layer "configured to provide non-bonding surfaces for the bumped contacts". In addition, dependent claim 50 recites the outer layer comprises "a conductive polymer". Fjelstad et al. teaches cap metals 34 which comprise an etch resistant metal. However, there is no teaching of a non-bonding metal, or of a conductive polymer for providing non-bonding surfaces.

Kazle was cited as teaching a conductive polymer 140a to provide a non-bonding surface. However, the conductive polymer 140a functions to provide a bonded connection with the bond pads 12a (column 4, lines 63-67). The use of a conductive polymer in Kazle is directly opposite to the presently claimed non-bonding function. Kazle teaches that solder and gold have been used to provide bonded connections (column 1, lines 34-44 and column 5, line 5 of Kazle). This teaching was apparently used by the Examiner to support the proposed combination of Kazle with Fjelstad

et al. and Maruyama et al. However, this position distorts the teachings of Kazle. As with the combination of Fjelstad et al. and Maruyama et al., the addition of Kazle with these references appears to have been reverse engineered for the purpose of supporting a rejection under 35 USC §103.

With regard to the conductive polymer, the Office Action further states: "to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice because applicants have not disclosed that a carbon film provides an advantage or solves a stated problem". This statement is incorrect, as page 13, lines 33-35 of the specification state that the conductive polymer provides a non-bonding surface.

The rejections of claims 40 and 41 over Kazle appear to be in error, as neither of these claims recites a conductive polymer. These 35 USC §103 rejections appear to have resulted from an improper cut and paste by the Examiner.

Conclusion


In view of the amendments and arguments, favorable consideration and allowance of claims 34, 35, 38-41, 43 and 49-51 is respectfully requested. In addition, rejoinder of withdrawn dependent claims 36, 37, 42 and 52 is requested.

Further, withdrawn claims 44-48 and 53-58 have been canceled. However, Applicant reserves the right to file the canceled claims in a separate divisional application.

Should any issues arise that will advance this case to allowance, the Examiner is asked to contact the undersigned by telephone.

DATED this 26th day of April, 2005.

Respectfully submitted:



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CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8

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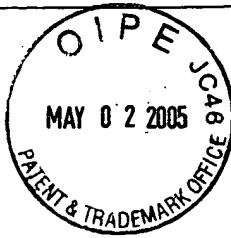
April 26, 2005
Date of Signature


Stephen A. Gratton, Attorney for Applicant

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

WARREN M. FARNWORTH
SALMAN AKRAM



Serial No.: 09/844,532

EXAMINER: Chang, R.

Filing Date: April 30, 2001

Art Unit: 3729

For: METHOD FOR FABRICATING A TEST INTERCONNECT
FOR BUMPED SEMICONDUCTOR COMPONENTS BY
FORMING RECESSES AND CANTILEVERED LEADS ON
A SUBSTRATE (AS AMENDED)

Attorney Docket No. 97-1433.1

INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR §1.56
April 30, 2004

Mail Stop NON FEE AMENDMENT
Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Sir:

The citations listed on the accompanying Form PTO/SB/08, copies attached, may be material to the examination of the subject application and are therefore submitted in compliance with the duty of disclosure defined in 37 CFR §§1.56, 1.97 and 1.98.

This Information Disclosure Statement under 37 CFR §§1.56, 1.97 and 1.98 is not to be construed as a representation that a search has been made, that additional material to the examination of this application does not exist, or that any one or more of these citations constitutes prior art under 35 USC §102.

It is requested that the above citations be made of record, if appropriate, in the prosecution of this application.

Respectfully submitted:

Stephen A. Gratton, Reg. No. 28,418
Attorney of Record

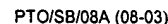
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April 30, 2004
Date of Signature

Stephen A. Gratton, Attorney for Applicants



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Sheet	1	of	1
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Application Number	09/844,532
Filing Date	04/30/2001
First Named Inventor	WARREN M. FARNWORTH
Art Unit	3729
Examiner Name	CHANG, R.
Attorney Docket Number	97-1433.1

U. S. PATENT DOCUMENTS

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FOREIGN PATENT DOCUMENTS

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Examiner Signature		Date Considered	
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This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

WARREN M. FARNWORTH
SALMAN AKRAM



Serial No.: 09/844,532

ART UNIT: 3729

Filing Date: 04/30/2001

EXAMINER: CHANG, R.

FOR: TEST INTERCONNECT FOR BUMPED
SEMICONDUCTOR COMPONENTS
AND METHOD OF FABRICATION

Docket No. 97-1433.1

**TRANSMITTAL OF INFORMATION DISCLOSURE STATEMENT BEFORE MAILING DATE OF
EITHER FINAL ACTION OR NOTICE OF ALLOWANCE UNDER 37 C.F.R. §1.97(c)**

September 30, 2004

MAIL STOP AMENDMENT
Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Dear Sir:

1. The information disclosure statement transmitted herewith is being filed after three months of the filing date of this national application or the date of entry of the national stage as set forth in §1.491 in an international application or after the mailing date of the first Office Action on the merits, whichever event occurred last but before the mailing date of either:

- a. a Final Action under §1.113 or
- b. a Notice of Allowance under §1.311, whichever occurs first.

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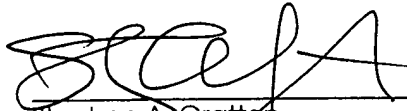
2. Accompanying this transmittal is
____ a certification as specified in 37 CFR 1.97(e).
 X the fee set forth in 37 CFR 1.17(p) for submission of an information disclosure statement under §1.97(c). (\$180.00).

X The commissioner is hereby authorized to charge payment of the following fees associated with this communication or credit any overpayment to

Deposit Account No. 07-1857, pertaining to i) any filing fees under 37 CFR 1.16 for the presentation of extra claims; ii) any patent application processing fees under 37 CFR 1.17.

DATED this 30th day of September, 2004.

Respectfully submitted:



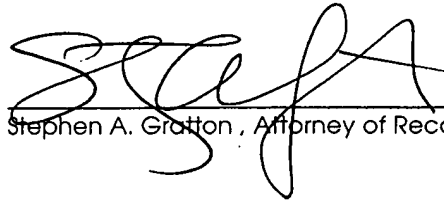
Stephen A. Gratton
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Date of Signature



Stephen A. Gratton, Attorney of Record

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September 30, 2004

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Stephen A. Gratton, Attorney of Record

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Application Number	09/844,532
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Sheet	1	of	2
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PTO/SB/08B (08-03)

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STATEMENT BY APPLICANT**

(Use as many sheets as necessary)

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Art Unit	3729
Examiner Name	CHANG, R.
Attorney Docket Number	97-1433.1

Sheet 2

of 2

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
	1	Information displayed at Chip Con 1997-1998, 4 sheets on FE CRD Floating Point Technology, (month unavailable).	

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¹ Applicant's unique citation designation number (optional). ² Applicant is to place a check mark here if English language Translation is attached. This collection of information is required by 37 CFR 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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SALMAN AKRAM



Serial No. 09/844,532

ART UNIT: 3729

Filing Date: APRIL 30, 2001

EXAMINER: CHANG, R.

FOR: METHOD FOR FABRICATING A TEST INTERCONNECT
FOR BUMPED SEMICONDUCTOR COMPONENTS BY FORMING
RECESSES AND CANTILEVERED LEADS ON A SUBSTRATE

Docket No. 97-1433.1

TRANSMITTAL OF INFORMATION DISCLOSURE STATEMENT BEFORE MAILING DATE OF
EITHER FINAL ACTION OR NOTICE OF ALLOWANCE UNDER 37 C.F.R. §1.97(c)

December 3, 2004

Mail Stop Amendment

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Dear Sir:

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- b. a Notice of Allowance under §1.311, whichever occurs first.

CERTIFICATE OR FEE

2. Accompanying this transmittal is

___ a certification as specified in 37 CFR 1.97(e).

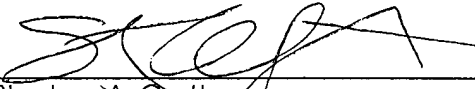
X the fee set forth in 37 CFR 1.17(p) for submission of an information disclosure statement under §1.97(c). (\$180.00).

X The commissioner is hereby authorized to charge payment of the following fees associated with this communication or credit any overpayment to

Deposit Account No. 07-1857, pertaining to i) any filing fees under 37 CFR 1.16 for the presentation of extra claims; ii) any patent application processing fees under 37 CFR 1.17.

DATED this 3rd day of December, 2004.

Respectfully submitted:



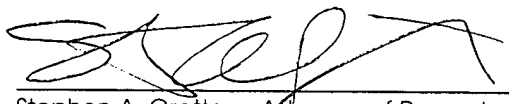
Stephen A. Gratton
Registration No. 28,418
Attorney of Record

2764 South Braun Way
Lakewood, CO 80228
Telephone: (303) 989 6353
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CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail, postage prepaid, in an envelope addressed to: MAIL STOP AMENDMENT, Commissioner for Patents, PO Box 1450, Alexandria, VA 22313-1450, on this 3rd day of December, 2004.

November 24, 2004
Date of Signature

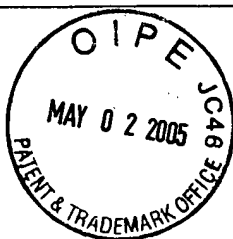


Stephen A. Gratton, Attorney of Record

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

WARREN M. FARNWORTH
SALMAN AKRAM



Serial No. 09/844,532

ART UNIT: 3729

Filing Date: APRIL 30, 2001

EXAMINER: CHANG, R.

FOR: METHOD FOR FABRICATING A TEST INTERCONNECT
FOR BUMPED SEMICONDUCTOR COMPONENTS BY FORMING
RECESSES AND CANTILEVERED LEADS ON A SUBSTRATE

Docket No. 97-1433.1

INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR §1.56
DECEMBER 3, 2004

Mail Stop Amendment
Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Sir:

The citations listed on the accompanying Form PTO/SB/08, copies attached, may be material to the examination of the subject application and are therefore submitted in compliance with the duty of disclosure defined in 37 CFR §§1.56, 1.97 and 1.98.

This Information Disclosure Statement under 37 CFR §§1.56, 1.97 and 1.98 is not to be construed as a representation that a search has been made, that additional material to the examination of this application does not exist, or that any one or more of these citations constitutes prior art under 35 USC §102.

It is requested that the above citations be made of record, if appropriate, in the prosecution of this application.

Respectfully submitted:

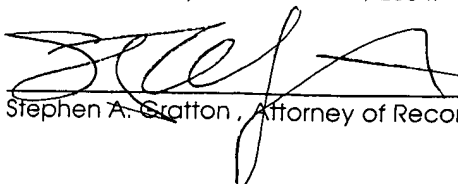

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December 3, 2004
Date of Signature


Stephen A. Gratton, Attorney of Record

